AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A static random access memory (SRAM) device comprising:

a first transistor pair coupled between a supply voltage line and GROUND;

a second transistor pair coupled between the supply voltage line and GROUND, the supply voltage line to receive a first supply voltage based on ~~a first~~ an ACTIVE mode of the memory device and to receive a second supply voltage based on a ~~second~~ STANDBY mode of the memory device, the second supply voltage being different than the first supply voltage;

a first access transistor coupled to a word line, a first bit line and a common node of the second transistor pair;

a second access transistor coupled to the word line, a second bit line and a common node of the first transistor pair; and

a bias transistor coupled to a body of one of the transistors of the first transistor pair and to a body of one of the transistors of the second transistor pair, the bias transistor to apply a forward body bias to the one transistor of the first transistor pair and to the one transistor of the second transistor pair based on ~~a non-ACTIVE mode/state~~ the memory device being in the STANDBY mode.

2. (Original) The SRAM device of claim 1, wherein the bias transistor comprises an NMOS transistor having a source coupled to GROUND.

3. (Previously Presented) The SRAM device of claim 2, wherein a drain of the bias transistor is coupled to the body of the one transistor of the first transistor pair and to the body of the one transistor of the second transistor pair.

4. (Currently Amended) The SRAM device of claim 1, wherein the bias transistor applies the forward body bias to the one transistor of the first transistor pair and to the one transistor of the second transistor pair ~~based on a mode of~~ when the memory device is in a STANDBY mode.

5. (Canceled)

6. (Currently Amended) The SRAM device of claim 1, wherein a gate of the bias transistor is coupled to a signal line to receive a STANDBY signal indicative of [[a]]the STANDBY ~~state~~ mode of the memory device.

7. (Original) The SRAM device of claim 1, wherein the bias transistor turns ON based on a STANDBY signal applied to a gate of the bias transistor.

8. (Original) The SRAM device of claim 1, wherein the one transistor of the first transistor pair comprises a PMOS transistor and the one transistor of the second transistor pair comprises another PMOS transistor.

9. (Currently Amended) A static random access memory (SRAM) device comprising:

a first SRAM memory cell having a cross-coupled inverter configuration, the cross-coupled inverter configuration including at least four transistors;

a supply voltage line to provide a first supply voltage to two transistors of the at least four transistors of the first SRAM memory cell ~~based on a first mode of~~ when the first SRAM memory cell is in an ACTIVE mode and to provide a second supply voltage to the two transistors ~~based on a second mode of~~ when the first SRAM memory cell is in a STANDBY mode, the second supply voltage being different than the first supply voltage; and

a switching device to apply a forward body bias to the two transistors of the cross-coupled inverter configuration of the first SRAM memory cell when the first SRAM memory cell is in the STANDBY mode.

10. (Currently Amended) The SRAM device of claim 9, further comprising a power control unit to change the supply voltage on the supply voltage line based on either the ~~first~~ ACTIVE mode or the ~~second~~ STANDBY mode of the first SRAM memory cell.

11. (Currently Amended) The SRAM device of claim 10, wherein the power control unit further to control switching of the switching device based on either the ~~first~~ ACTIVE mode or the ~~second~~ STANDBY mode of the first SRAM memory cell.

12. (Original) The SRAM device of claim 10, wherein the switching device comprises an NMOS transistor having a source coupled to GROUND and a gate coupled to the power control unit.

13. (Previously Presented) The SRAM device of claim 12, wherein a drain of the NMOS transistor is coupled to a body of each of the two transistors of the at least four transistors of the first SRAM memory cell.

14. (Currently Amended) The SRAM device of claim 12, wherein a gate of the NMOS transistor receives a STANDBY signal from the power control unit indicative of [[a]]the STANDBY ~~state~~ mode of the first SRAM memory cell.

15. (Previously Presented) The SRAM device of claim 12, wherein the NMOS transistor turns ON based on a STANDBY signal applied to the gate of the NMOS transistor.

16. (Previously Presented) The SRAM device of claim 9, further comprising a second SRAM memory cell having a cross-coupled inverter configuration, the cross-

coupled inverter configuration of the second SRAM memory cell including at least four transistors, the supply voltage line to provide a supply voltage to two transistors of the at least four transistors of the second SRAM memory cell based on a mode of the second SRAM memory cell.

17. (Previously Presented) The SRAM device of claim 16, wherein the switching device to apply a forward body bias to the two transistors of the at least four transistors of the cross-coupled configuration of the second SRAM memory cell.

18. (Currently Amended) An electronic system comprising:

a processor device to process data;

a static random access memory (SRAM) device to store the data; and

a power control unit to control a supply voltage level applied to the SRAM device and to provide a signal indicative of a mode of the SRAM device, the power control unit to apply a first voltage level when the SRAM device is in ~~a first~~ an ACTIVE mode and to apply a second voltage level when the SRAM device is in a ~~second~~ STANDBY mode, the SRAM device including:

a switching device to apply a forward bias to transistors within the SRAM device based on the signal provided by the power control unit indicative of ~~either~~ the ~~first mode or the second~~ STANDBY mode of the SRAM device.

19. (Original) The electronic system of claim 18, wherein the switching device applies the forward body bias by coupling a body of each of the transistors to GROUND.

20. (Original) The electronic system of claim 18, wherein applying the forward bias to the transistors increases a static noise margin.

21-23. (Canceled)

24. (Currently Amended) The electronic system of claim [[23]]18, wherein the power control unit to provide the supply voltage level to two transistors of the SRAM device in both the STANDBY mode and the ACTIVE mode.

25. (Previously Presented) The electronic system of claim 24, wherein the SRAM device further including a device to couple bodies of the two transistors of a memory cell in the SRAM device to a supply voltage line when the memory cell is not in the STANDBY mode.

26. (Previously Presented) The SRAM device of claim 17, wherein the switching device to apply the forward body bias to the two transistors of the at least four transistors of the second SRAM memory cell when the second SRAM memory cell is in a STANDBY mode.

27-28. (Canceled)

29. (Currently Amended) The SRAM device of claim [[28]]9, further comprising a device to couple bodies of the two transistors of the at least four transistors to the supply voltage line when the first SRAM memory cell is not in the STANDBY mode.

30. (Currently Amended) The SRAM device of claim 1, wherein the supply voltage line applies the first supply voltage in the ~~first~~ ACTIVE mode and applies the second supply voltage in the ~~second~~ STANDBY mode.

31-32. (Canceled)

33. (Currently Amended) The SRAM device of claim [[32]]1, wherein the supply voltage line to provide a supply voltage to the one transistor of the first transistor pair and the one transistor of the second transistor pair in both the STANDBY mode and the ACTIVE mode.

34. (Previously Presented) The SRAM device of claim 33, further comprising a device to couple bodies of the two transistors to the supply voltage line when a memory cell of the SRAM device is not in the STANDBY mode.

35. (Previously Presented) The SRAM device of claim 1, wherein the first supply voltage and the second supply voltage are applied to a source of the one transistor of the first transistor pair and to a source of the one transistor of the second transistor pair.

36. (Previously Presented) The SRAM device of claim 9, wherein the supply voltage line to provide the first supply voltage and the second supply voltage to sources of the two transistors of the at least four transistors of the first SRAM memory cell.

37. (Previously Presented) The electronic system of claim 18, wherein the power control unit to apply the first voltage level and the second voltage level to sources of transistors within the SRAM device.